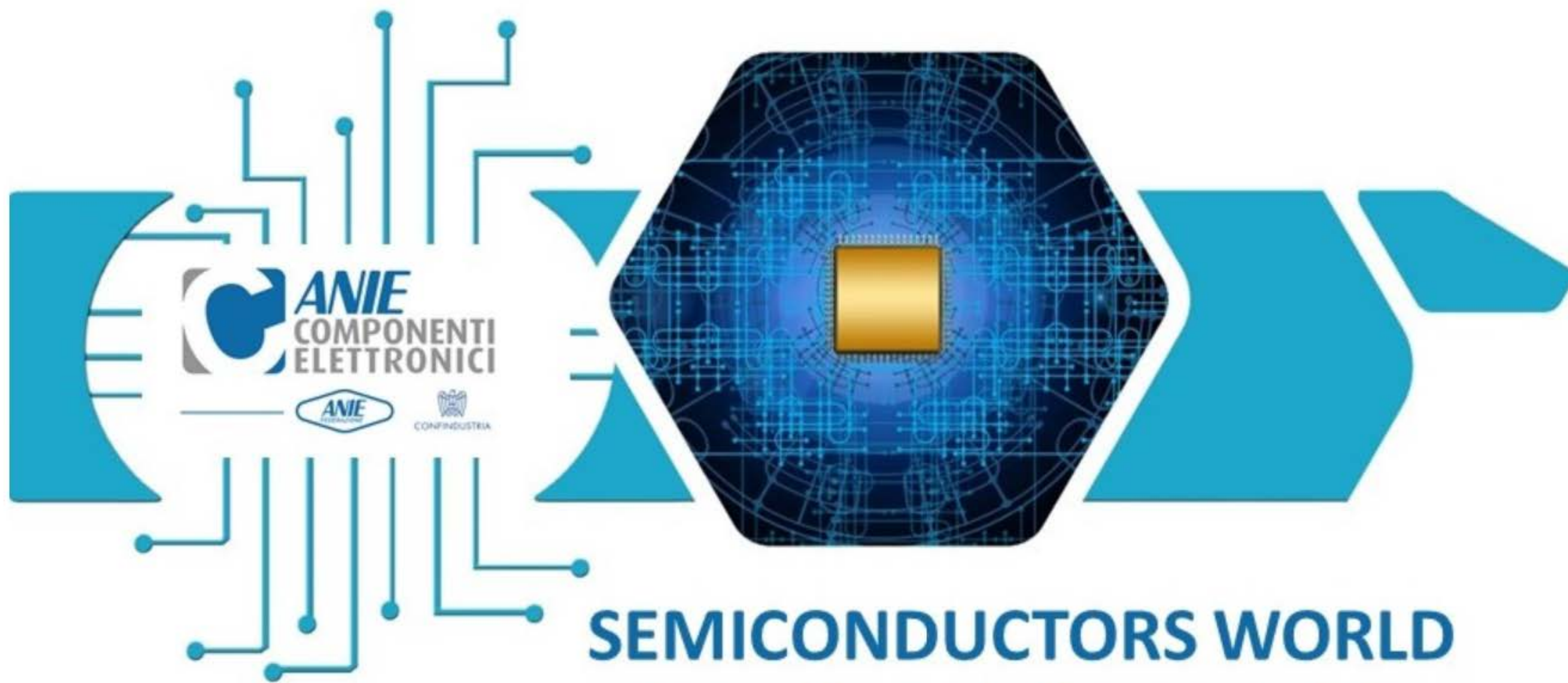


Gabriele Braga

Managing Board
ANIE Componenti Elettronici

ANIE COMPONENTI ELETTRONICI

ANIE FEDERAZIONE CONFINDUSTRIA

Agenda

- Costruire un semiconduttore: ciclo produttivo e materie prime
- Scenario del mercato
- Vulnerabilità e recenti accadimenti
- L’innovazione e la progettazione: il paradosso Lego sull’integrazione e specializzazione
- Autosufficienza: risorse economiche, temporali ed umane
- Proteggersi dalla situazione congiunturale

Costruire un semiconduttore: ciclo produttivo e materie prime

Sand

With about 25% (mass) Silicon is – after Oxygen – the second most frequent chemical element in the earth's crust. Sand – especially Quartz - has high percentages of Silicon in the form of Silicon dioxide (SiO_2) and is the base ingredient for semiconductor manufacturing.

Melted Silicon –

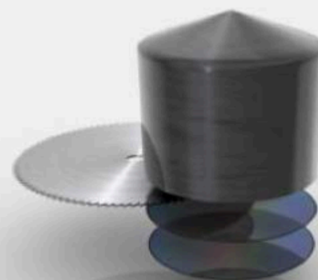
scale: wafer level (~300mm / 12 inch)

Silicon is purified in multiple steps to finally reach semiconductor manufacturing quality which is called Electronic Grade Silicon. Electronic Grade Silicon may only have one alien atom every one billion Silicon atoms. In this picture you can see how one big crystal is grown from the purified silicon melt. The resulting mono crystal is called an Ingot.

Mono-crystal Silicon Ingot –

scale: wafer level (~300mm / 12 inch)

An ingot has been produced from Electronic Grade Silicon. One ingot weights about 100 kilograms (=220 pounds) and has a Silicon purity of 99.9999999%



Ingot Slicing –

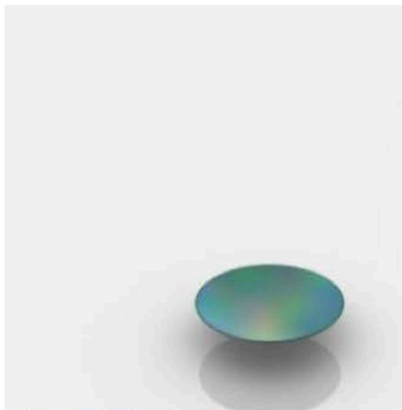
scale: wafer level (~300mm / 12 inch)

The Ingot is cut into individual silicon discs called wafers. The thickness of a wafer is about 1mm.

Wafer –

scale: wafer level (~300mm / *12 inch*)

The wafers are polished until they have flawless, mirror-smooth surfaces. Intel buys those manufacturing ready wafers from third party companies. Intel's highly advanced 32nm High-K/Metal Gate process uses wafers with a diameter of 300 millimeter (~12 inches). When Intel first began making chips, the company printed circuits on 2-inch (50mm) wafers. Now the company uses 300mm wafers, resulting in decreased costs per chip.



Applying Photo Resist –

scale: wafer level (~300mm / 12 inch)

Fabrication of chips on a wafer consists of hundreds of precisely controlled steps which result in a series of patterned layers of various materials one on top of another. What follows is a sample of the most important steps in this complex process. In this image there's photo resist (blue color) applied, exposed and exposed photo resist is being washed off before the next step (more details later). The remaining photo resist (blue shine on wafer) will protect material that should not get ions implanted.

Ion Implantation –

scale: wafer level (~300mm / 12 inch)

The wafer is patterned using photolithography (details of how this is done will be described later). The wafer is bombarded with a beam of ions (positively or negatively charged atoms) which embed themselves beneath the surface of the wafer to alter the conductive properties of the silicon in selected locations. The green regions in the image to the right have these implanted alien atoms.

Removing Photo Resist –

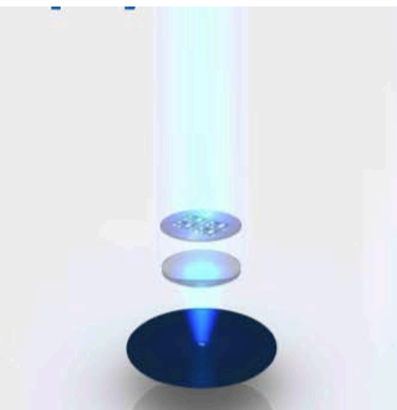
scale: wafer level (~300mm / 12 inch)

After the ion implantation the photo resist will be removed and the material that should have been doped (green) has alien atoms implanted now (notice slight variations in color)

Applying Photo Resist –

scale: wafer level (~300mm / 12 inch)

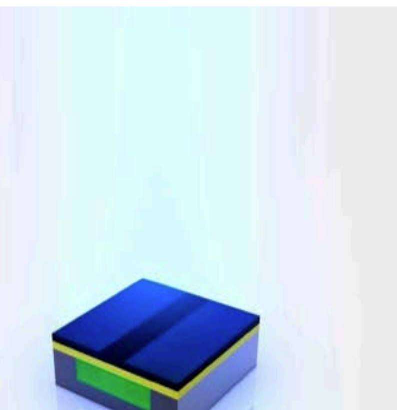
The liquid (dark color here) that's poured onto the wafer while it spins is a photo resist finish similar as the one known from film photography. The wafer spins during this step to allow very thin and even application of this photo resist layer.



Exposure –

scale: wafer level (~300mm / 12 inch)

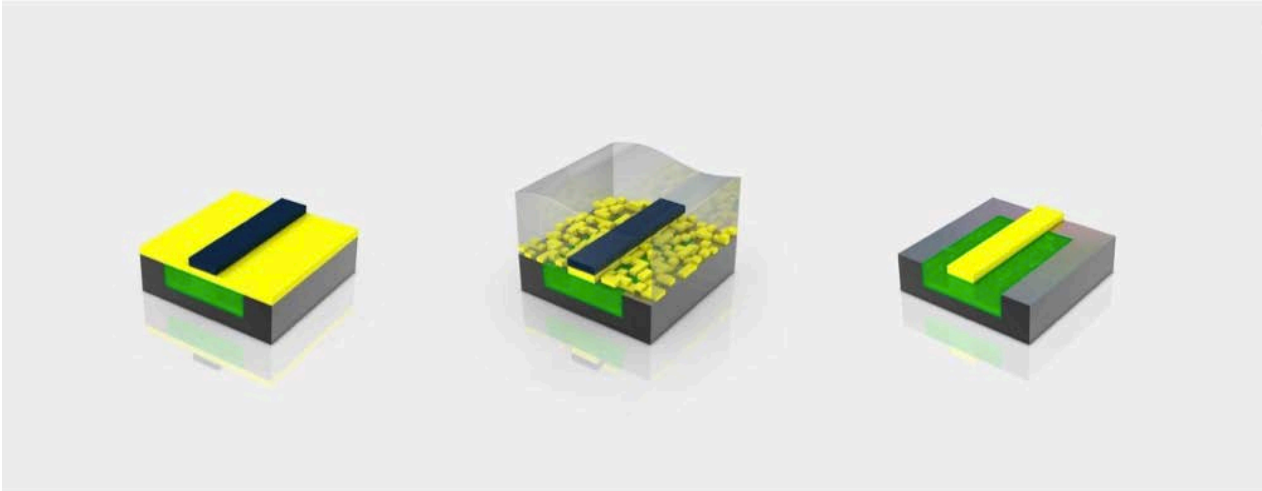
The photo resist finish is exposed to ultra violet (UV) light. The chemical reaction triggered by that process step is similar to what happens to film material in a film camera the moment you press the shutter button. The photo resist finish that's exposed to UV light will become soluble. The exposure is done using masks that act like stencils in this process step. When used with UV light, masks create the various circuit patterns on each layer of the microprocessor. A lens (middle) reduces the mask's image. So what gets printed on the wafer is typically four times smaller linearly than the mask's pattern.



Exposure –

scale: transistor level (~50-200nm)

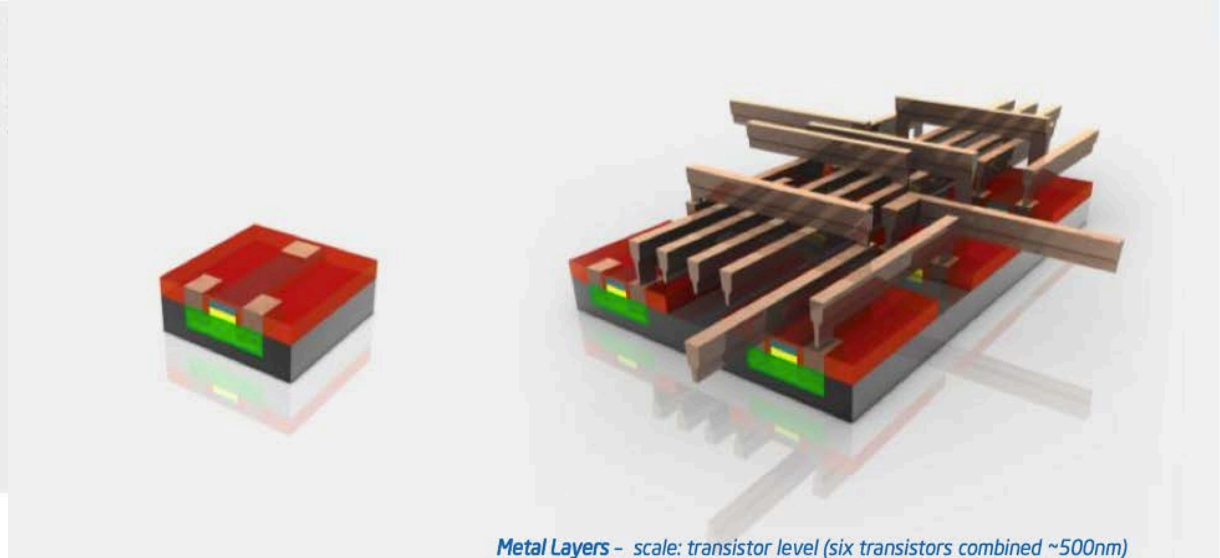
Although usually hundreds of microprocessors are built on a single wafer, this picture story will only focus on a small piece of a microprocessor from now on – on a transistor or parts thereof. A transistor acts as a switch, controlling the flow of electrical current in a computer chip. Intel researchers have developed transistors so small that about 30 million of them could fit on the head of a pin.



Washing off of Photo Resist –
scale: transistor level (~50-200nm)
The gooey photo resist is completely dissolved by a solvent. This reveals a pattern of photo resist made by the mask (dark rectangle here).

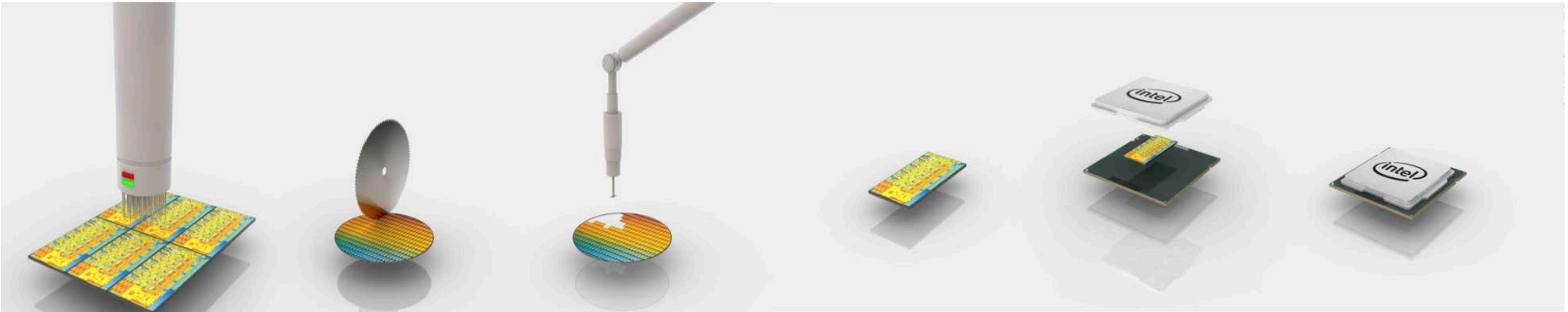
Etching –
scale: transistor level (~50-200nm)
The photo resist is protecting the high-k dielectric that should not be etched away. Revealed material will be etched away with chemicals.

Removing Photo Resist –
scale: transistor level (~50-200nm)
After the etching the photo resist is removed and the desired shape becomes visible.



Polishing –
scale: transistor level (~50-200nm)
The excess material is polished off.

Metal Layers – scale: transistor level (six transistors combined ~500nm)
Multiple metal layers are created to interconnect (think: wires) in between the various transistors. How these connections have to be "wired" is determined by the architecture and design teams that develop the functionality of the respective processor (e.g. Intel® Core™ i5 Processor). While computer chips look extremely flat, they may actually have over 30 layers to form complex circuitry. If you look at a magnified view of a chip, you will see an intricate network of circuit lines and transistors that look like a futuristic, multi-layered highway system.



Wafer Sort Test –

scale: die level (~10mm / ~0.5 inch)

This fraction of a ready wafer is being put to a first functionality test. In this stage test patterns are fed into every single chip and the response from the chip monitored and compared to "the right answer".

Wafer Slicing –

scale: wafer level (~300mm / 12 inch)

The wafer is cut into pieces (called dies). The above wafer contains 2nd generation Intel® Core™ i5 processors with integrated Intel HD Graphics.

Discarding faulty Dies –

scale: wafer level (~300mm / 12 inch)

The dies that responded with the right answer to the test pattern will be put forward for the next step (packaging).

Individual Die –

scale: die level (~10mm / ~0.5 inch)

These are individual dies which have been cut out in the previous step (slicing). The dies shown here are dies of a 2nd generation Intel® Core™ i5 Processor.

Packaging –

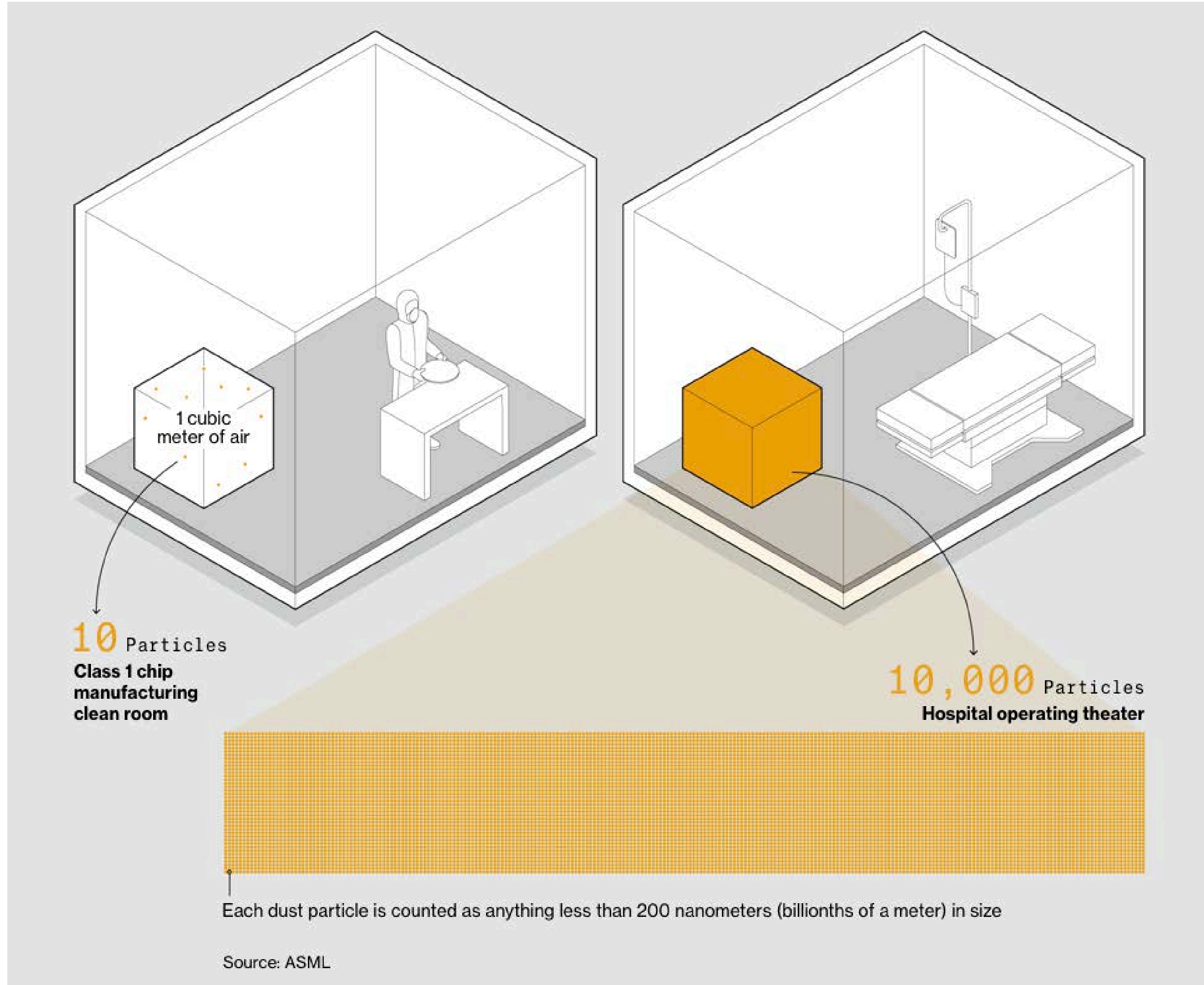
scale: package level (~20mm / ~1 inch)

The substrate, the die and the heatspreader are put together to form a completed processor. The green substrate builds the electrical and mechanical interface for the processor to interact with the rest of the PC system. The silver heatspreader is a thermal interface where a cooling solution will be put on to. This will keep the processor cool during operation.

Processor –

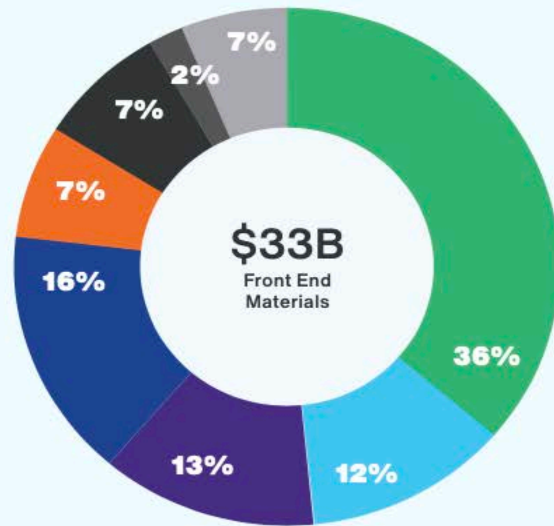
scale: package level (~20mm / ~1 inch)

Completed processor (2nd generation Intel® Core™ i5 Processor in this case). A microprocessor is the most complex manufactured product on earth. In fact, it takes hundreds of steps – only the most important ones have been visualized in this picture story - in the world's cleanest environment (a microprocessor fab) to make microprocessors.

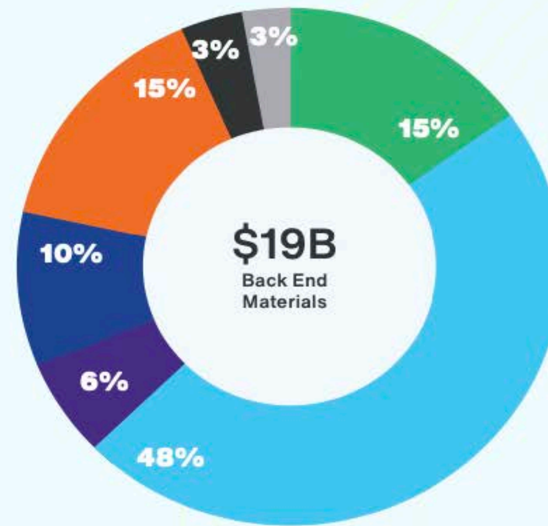

1 cubic
meter of air
10 Particles
Class 1 chip
manufacturing
clean room
10,000 Particles
Hospital operating theater
Each dust particle is counted as anything less than 200 nanometers (billionths of a meter) in size
Source: ASML

Breakdown of market size of semiconductor manufacturing materials, 2019 (% of $ Billion)

Front End (wafer fabrication)



Back End (assembly, packaging & testing)



Front End	Back End
Silicon wafers	Leadgrames
Photomask	Organic substrates
Photoresist and ancillary chemicals	Ceramic packages
Gases	Encapsulation resins
Wet chemicals	Bonding wire
CMP[1] slurries and pads	Die attach materials
Sputtering target	Others
Others	

1. Chemical-mechanichal planarization

Sources: BCG analysis based on data from SEMI, IHS and HSBC

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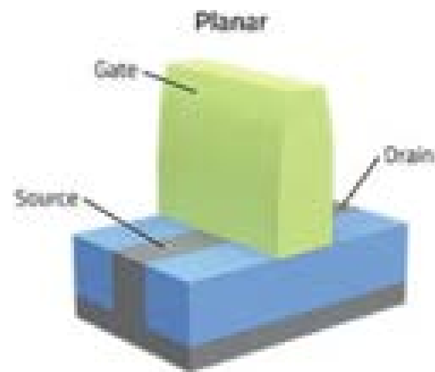
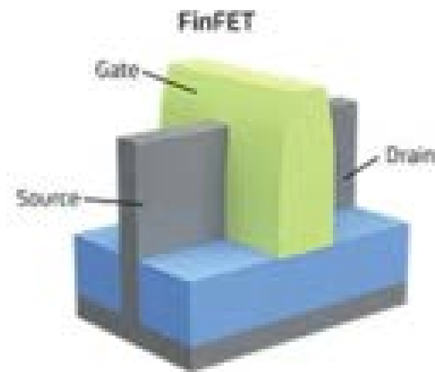
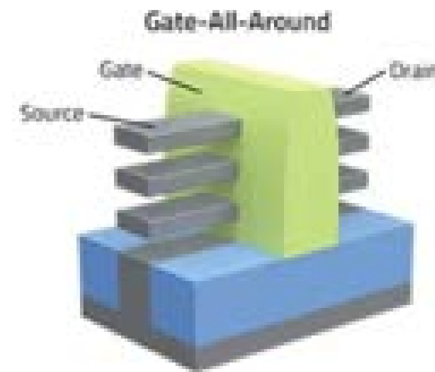
Le materie prime per costruire i semiconduttori







La metrica del livello tecnologico dei semiconduttori: i nanometri

Moore's Law: The number of transistors on microchips doubles every two years

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years.
This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

Transistor count

50,000,000,000
10,000,000,000
5,000,000,000
1,000,000,000
500,000,000
100,000,000
50,000,000
10,000,000
5,000,000
1,000,000
500,000
100,000
50,000
10,000
5,000
1,000

GC2 IPU
AMD Epyc Rome
72-core Xeon Phi
Centriq 2400
AWS Graviton2
SPARC M7
32-core AMD Epyc
IBM z13 Storage Controller
Apple A12X Bionic
18-core Xeon Haswell-E5
HiSilicon Kirin 990 5G
Apple A13 (iPhone 11 Pro)
Xbox One main SoC
61-core Xeon Phi
AMD Ryzen 7 3700X
12-core POWER8
HiSilicon Kirin 710
8-core Xeon Nehalem-EX
10-core Core i7 Broadwell-E
Six-core Xeon 7400
Qualcomm Snapdragon 835
Dual-core Itanium 2
Dual-core + GPU Iris Core i7 Broadwell-U
Quad-core + GPU GT2 Core i7 Skylake K
Pentium D Presler
POWER6
Quad-core + GPU Core i7 Haswell
Apple A7 (dual-core ARM64 "mobile SoC")
Itanium 2 with 9 MB cache
Core i7 (Quad)
AMD K10 quad-core 2M L3
Itanium 2 Madison 6M
Core 2 Duo Wolfdale
Pentium D Smithfield
Core 2 Duo Conroe
Itanium 2 McKinley
Cell
Core 2 Duo Wolfdale 3M
Pentium 4 Prescott-2M
Core 2 Duo Allendale
Pentium 4 Cedar Mill
AMD K8
Pentium 4 Prescott
Pentium 4 Northwood
Barton
Pentium 4 Willamette
Atom
Pentium III Tualatin
Pentium II Mobile Dixon
AMD K7
Pentium III Coppermine
ARM Cortex-A9
AMD K6-III
AMD K6
Pentium III Katmai
Pentium II Deschutes
Pentium Pro
Pentium II Klamath
Pentium
AMD K5
SA-110
Intel 80486
R4000
TI Explorer's 32-bit Lisp machine chip
ARM700
Intel 80386
Intel i960
ARM 3
Motorola 68020
DEC WRL MultiTitan
Intel 80286
ARM 9TDMI
Motorola 68000
Intel 80186
Intel 8086
Intel 8088
ARM 2
ARM 6
ARM 1
WDC 65C816
Motorola 6809
Novix NC4016
TMS 1000
Zilog Z80
WDC 65C02
RCA 1802
Intel 8085
Intel 8008
Intel 8080
MOS Technology 6502
Motorola 6800
Intel 4004

1970 1972 1974 1976 1978 1980 1982 1984 1986 1988 1990 1992 1994 1996 1998 2000 2002 2004 2006 2008 2010 2012 2014 2016 2018 2020

Year in which the microchip was first introduced

Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)
OurWorldinData.org – Research and data to make progress against the world's largest problems.

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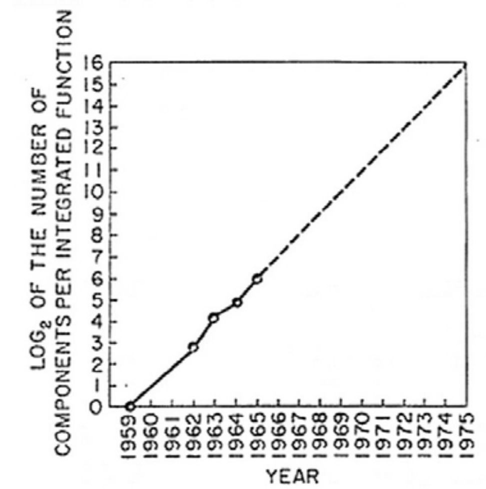

Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

La dinamica evolutiva: l'integrazione

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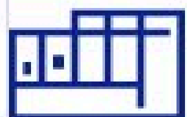


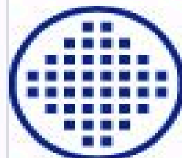
500+

Machines in a fab

Including lithography machines

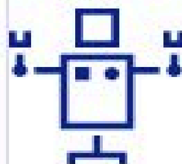
€15bn+

Cost of building a fab



50k

Average wafer starts per month



1,000+

Steps in chipmaking process

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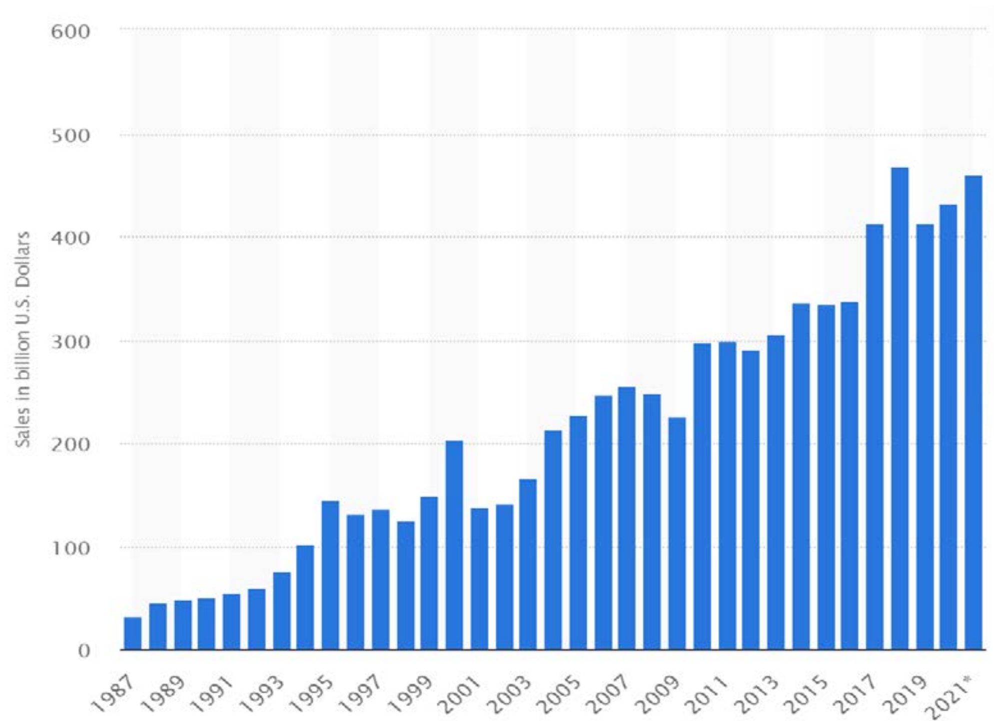
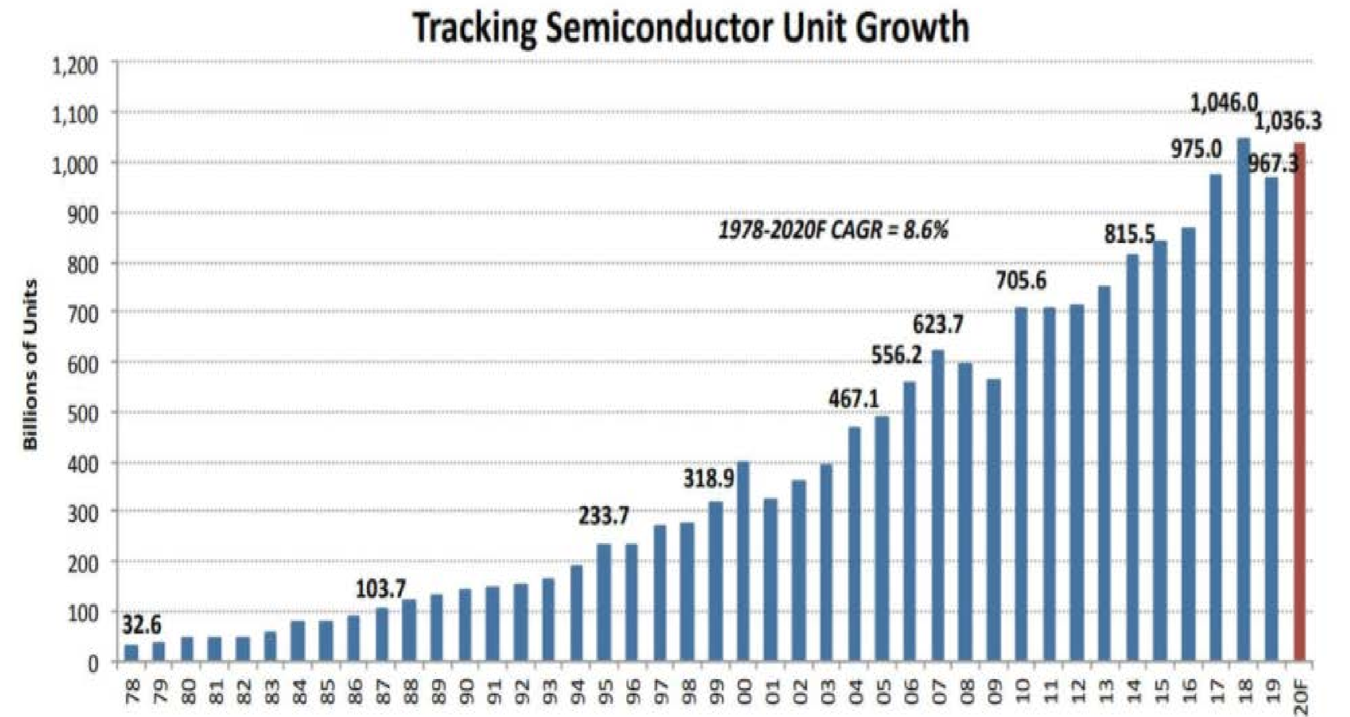
Scenario del mercato

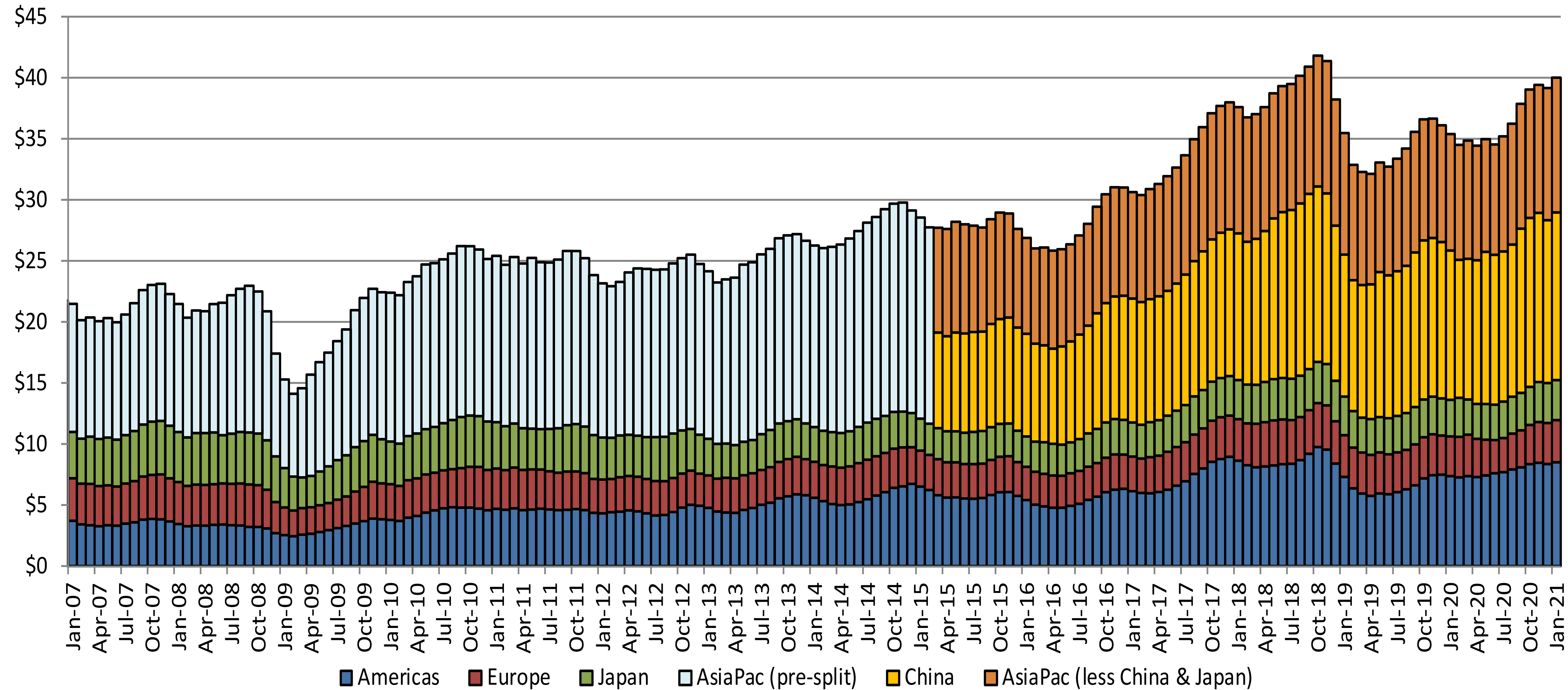
Digital transformation as a relentless journey





Monthly Billings Detail by Region

April 2019 was the most recent trough in Worldwide billings, peaking in November 2019. December 2019 through February 2020 were all down M/M. Since March 2020, the Worldwide billings have seen some volatility, January 2021 results up M/M.



Source: Semiconductor Industry Association (SIA) - 3 month rolling average billings

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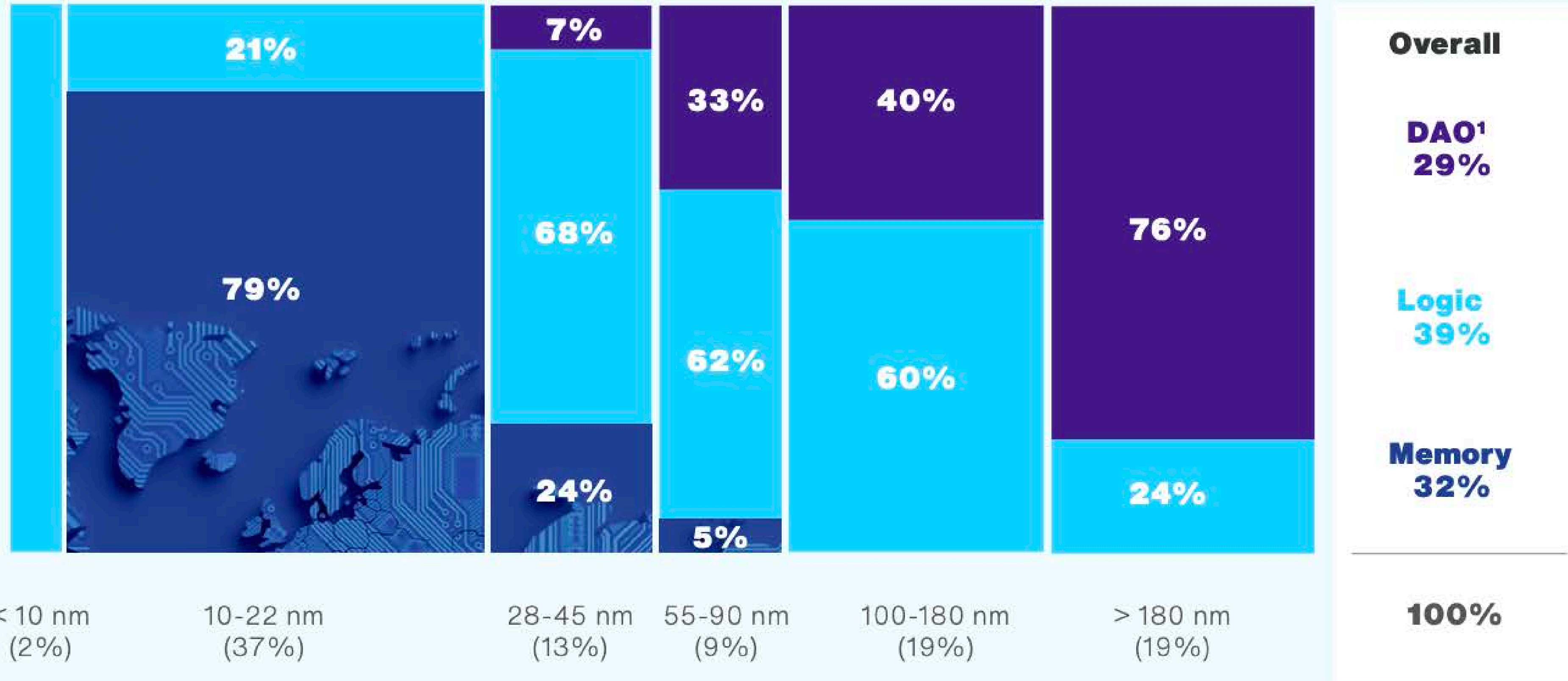
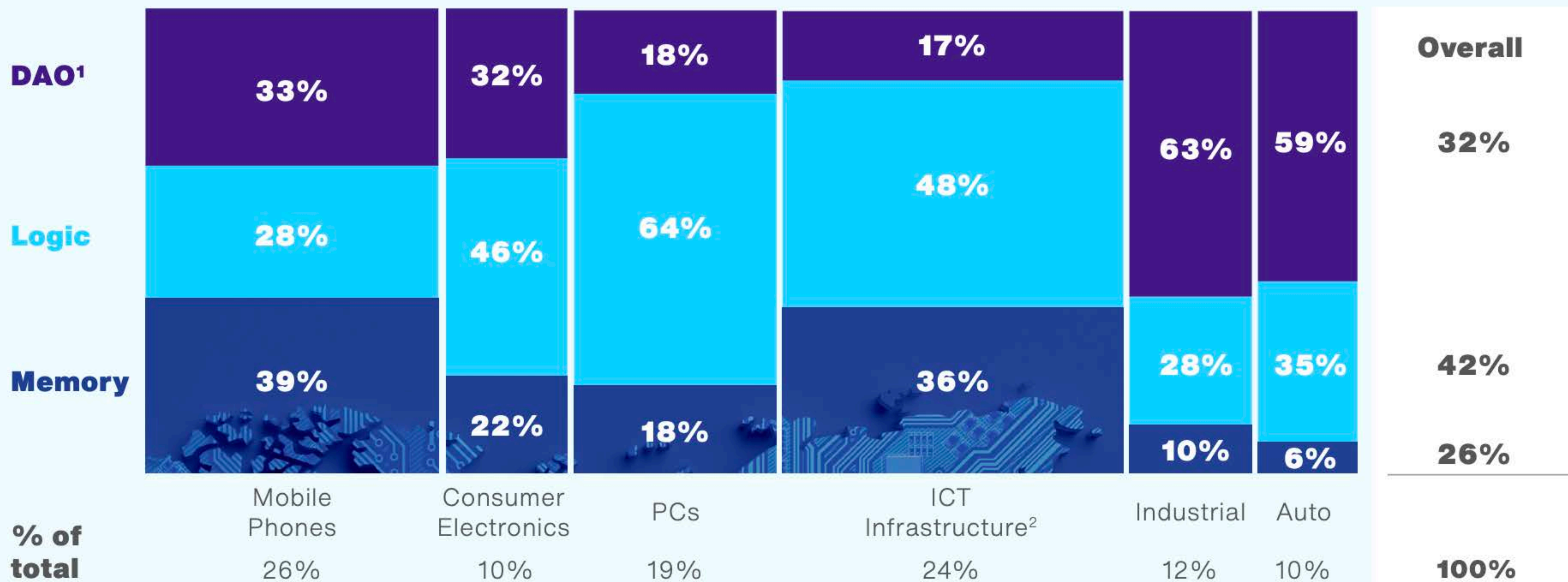
Tipologia di componenti: geometrie e mercati applicativi

Global manufacturing capacity by node and semiconductor type, 2019 (% of 8" equivalent wafers per month)



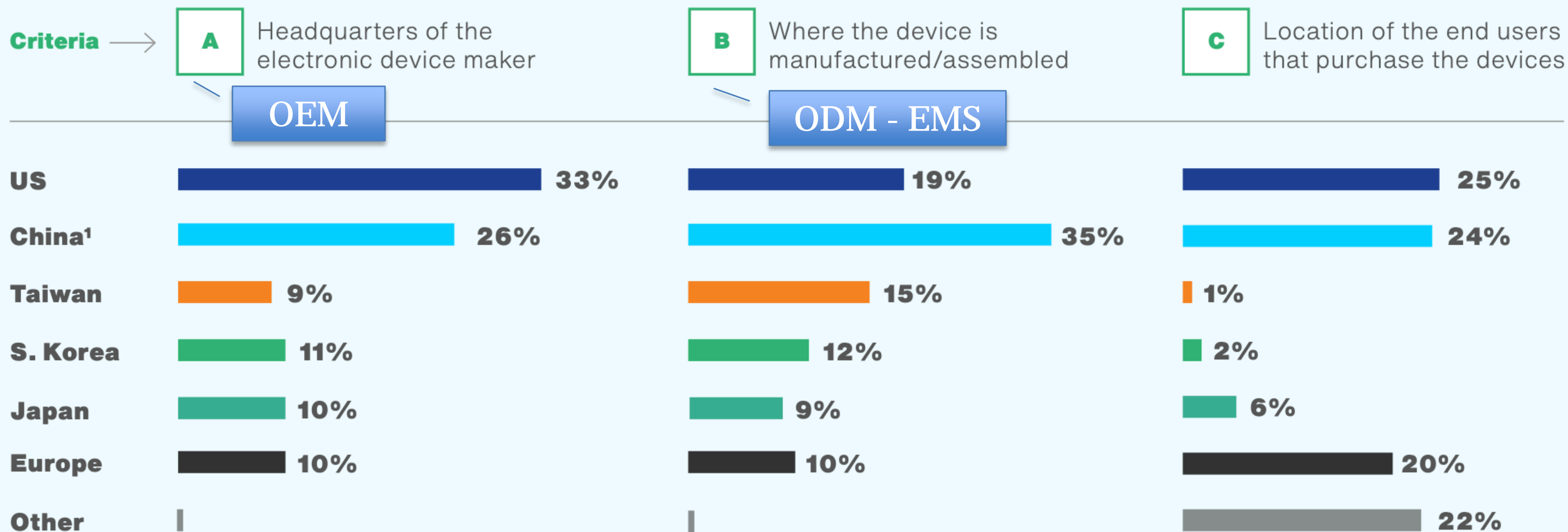
1. Discrete, analog and optoelectronics and sensors
Sources: BCG analysis based on SEMI data

Global semiconductor sales by application market, 2019 (%)



$412B
GLOBAL
2019 SALES

1. Discrete, analog and optoelectronics and sensors
2. Information and Communications Technology infrastructure, including data centers and communication networks
Sources: SIA WSTS, Gartner



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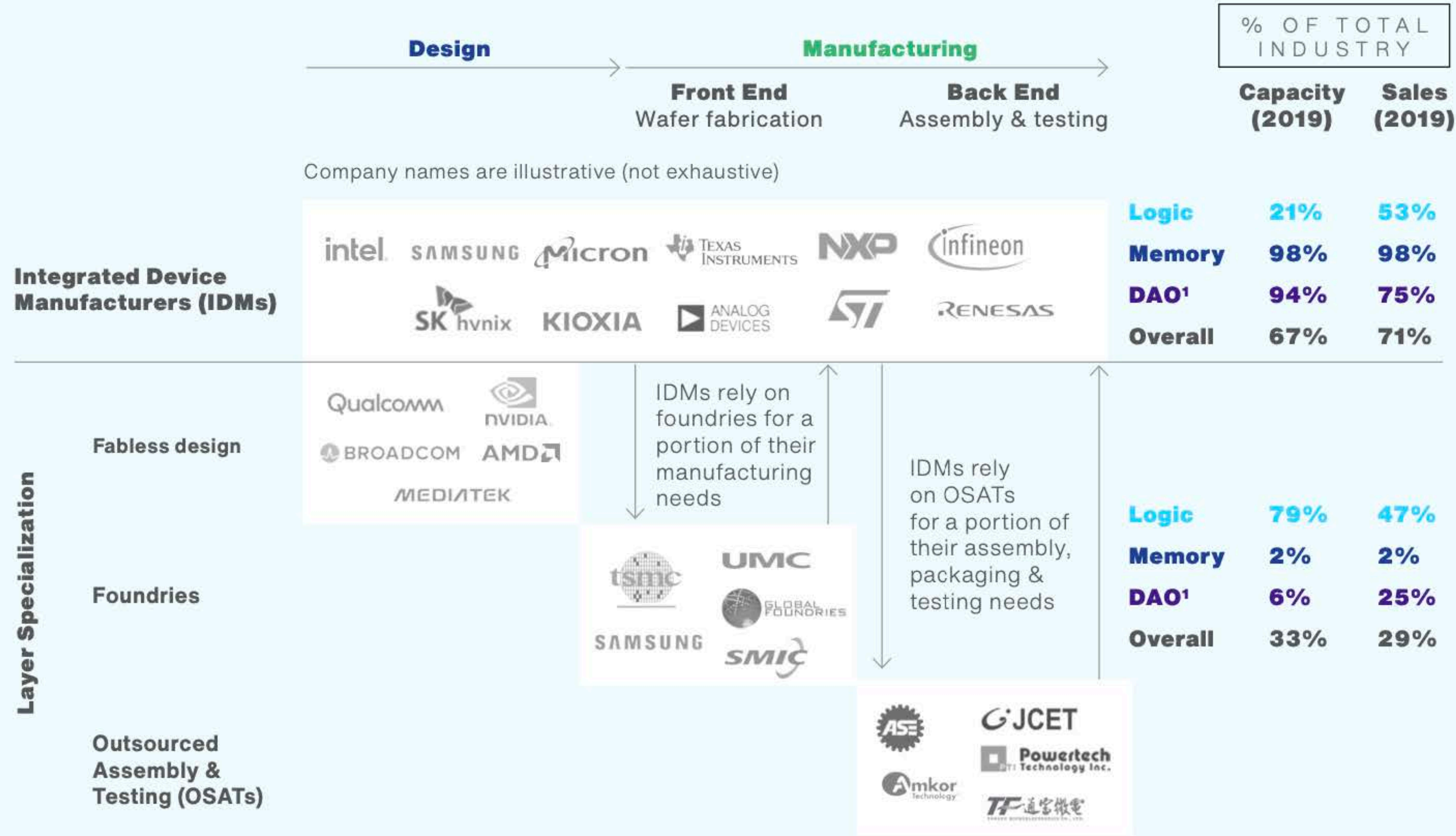
Modelli di business



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IDMs
Segment economics
(% of annual revenue, 2016-2019)

- Gross Margin: 52%
- R&D: 14%
- Capex: 20%
- Operating Cash Flow: 17%

Fabless
Segment economics
(% of annual revenue, 2016-2019)

- Gross Margin: 50%
- R&D: 20%
- Capex: 4%
- Operating Cash Flow: 20%

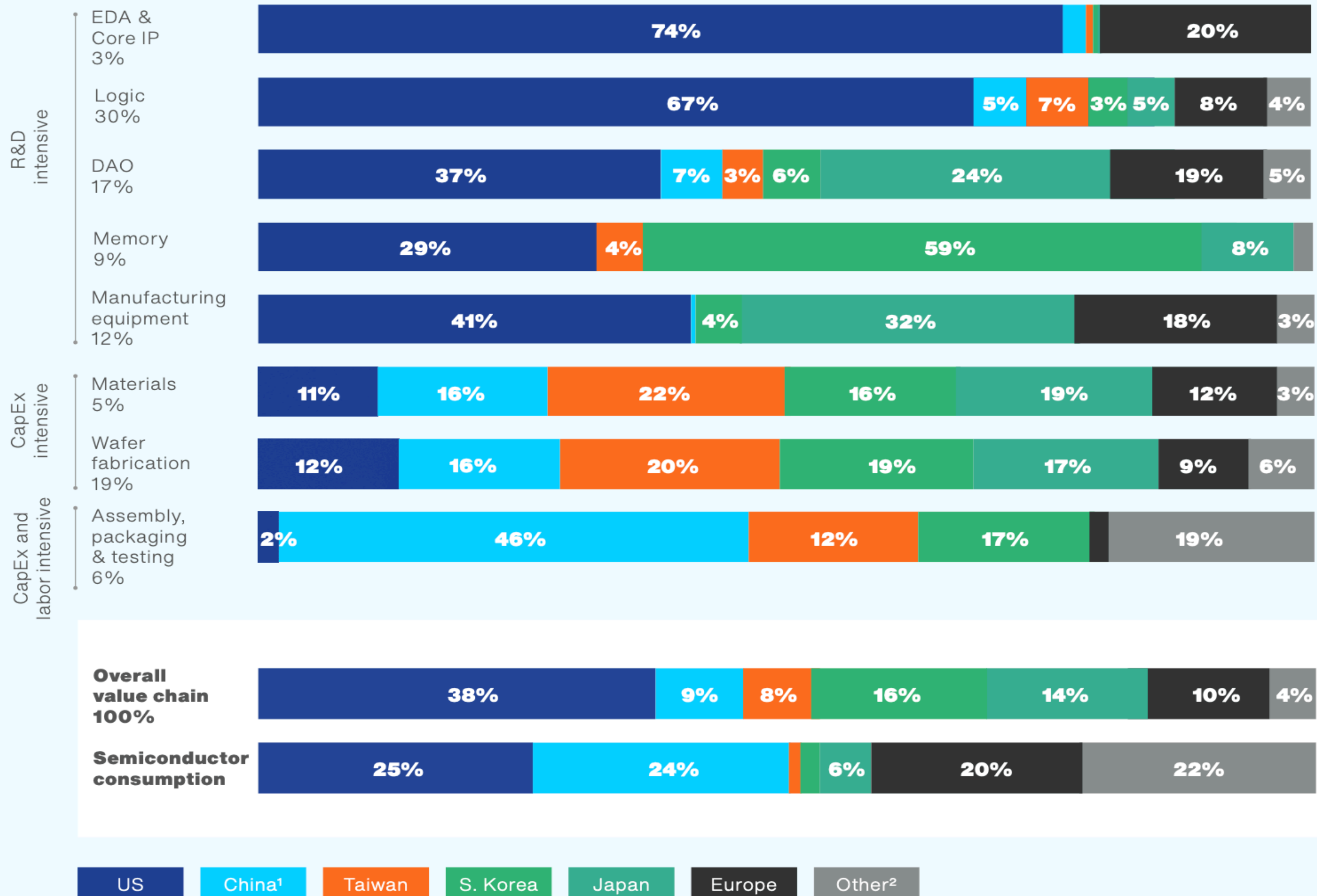
Foundries
Segment economics
(% of annual revenue, 2016-2019)

- Gross Margin: 40%
- R&D: 9%
- Capex: 34%
- Operating Cash Flow: 15%

OSATs
Segment economics
(% of annual revenue, 2016-2019)

- Gross Margin: 17%
- R&D: 4%
- Capex: 16%
- Operating Cash Flow: 2%

Regionalizzazione della value chain



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CONFINDUSTRIA

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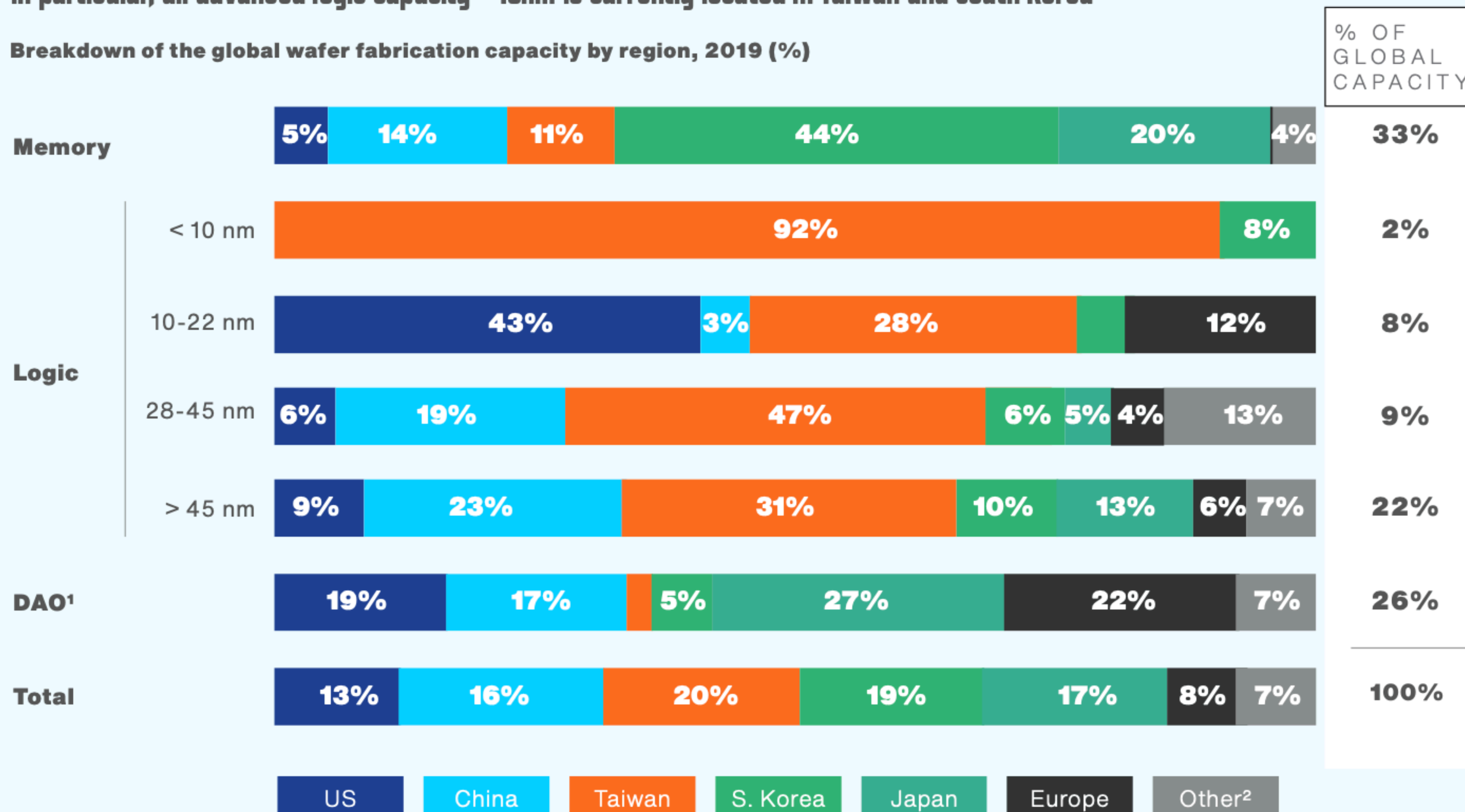
East Asia + China concentrate about 75% of the wafer fabrication capacity; in particular, all advanced logic capacity < 10nm is currently located in Taiwan and South Korea

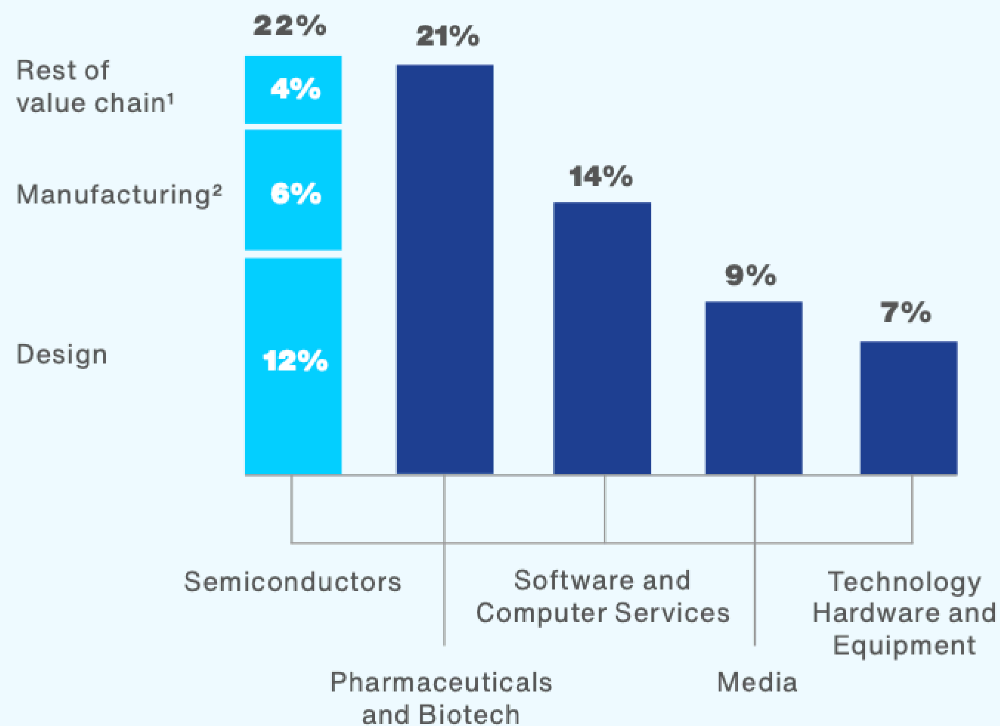


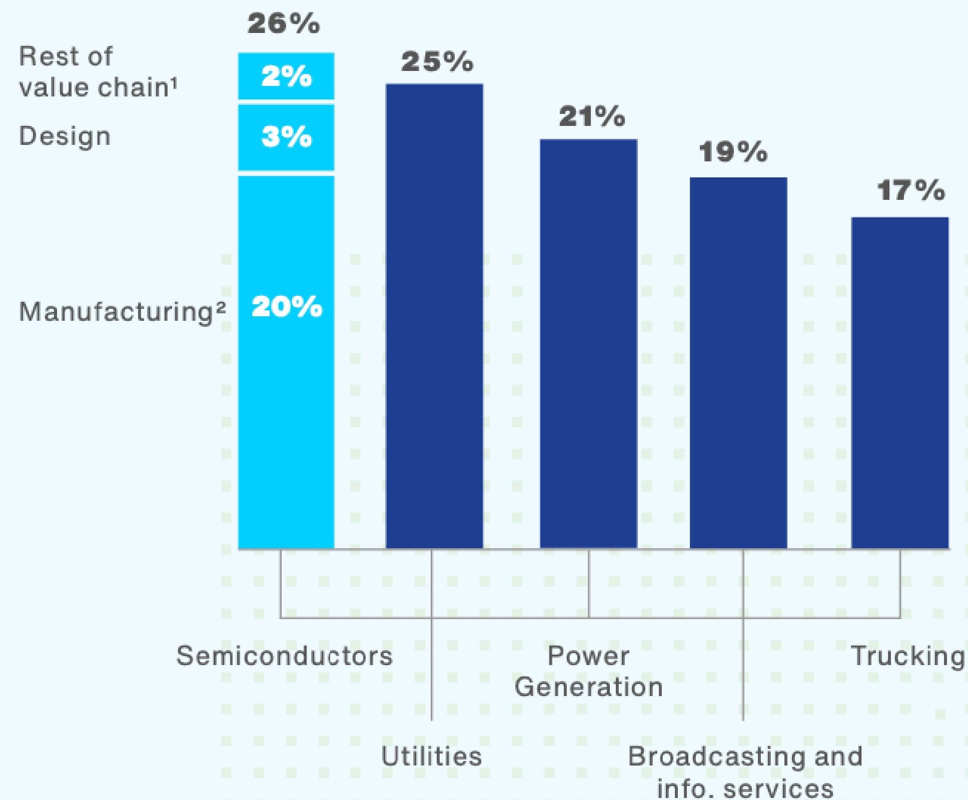
1. Discretes, analog and optoelectronics and sensors
2. Other includes Israel, Singapore and the rest of the world

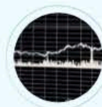
Sources: BCG analysis with data from SEMI fab database

Produttori e investitori

The semiconductor industry ranks high simultaneously in both R&D and capital intensity







1. Pre-competitive research
(15 to 20% of total industry R&D)

2. Design

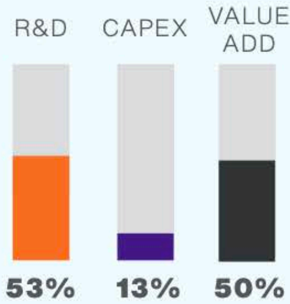
Manufacturing

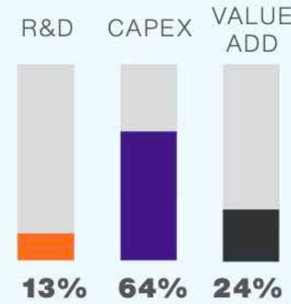
3. Front End
Wafer fabrication

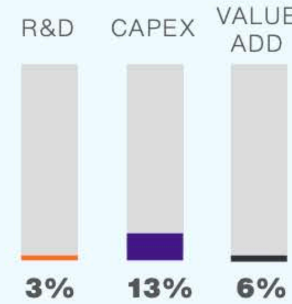
4. Back End
Assembly, packaging & testing

$ 412 B
GLOBAL
2019 SALES

% of industry total, 2019



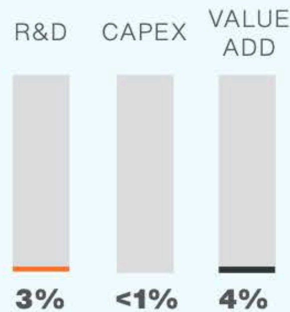


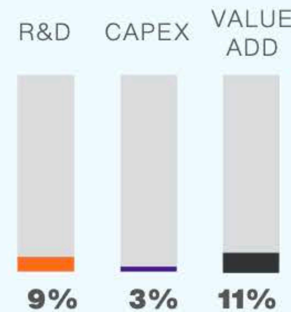


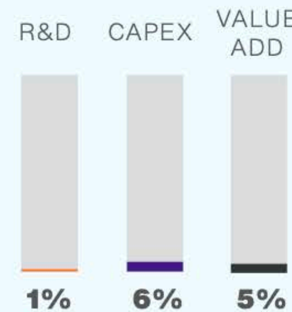
5. EDA & Core IP

6. Equipment & Tools

7. Materials







R&D
$92B

CAPEX
$108B

VALUE ADD
$290B

Electronic Devices

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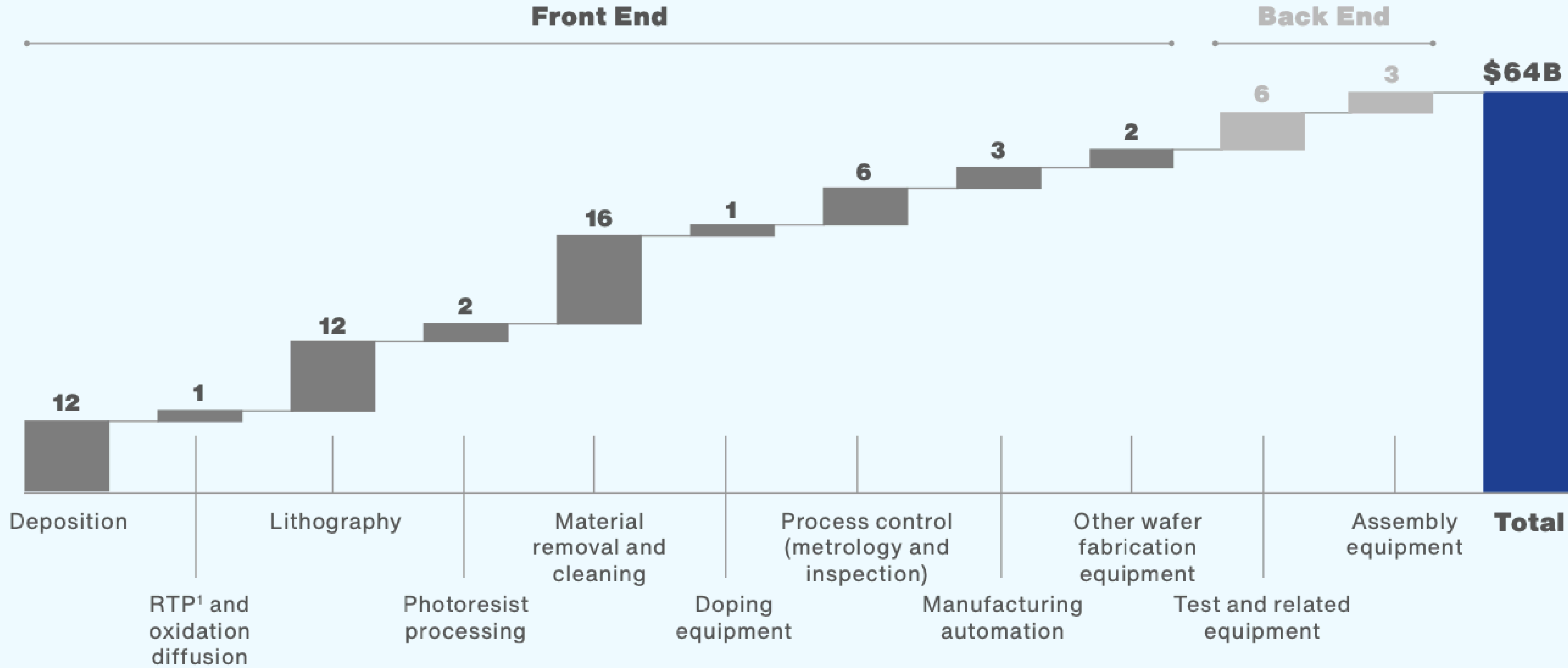

1. Rapid thermal processing
Sources: Gartner

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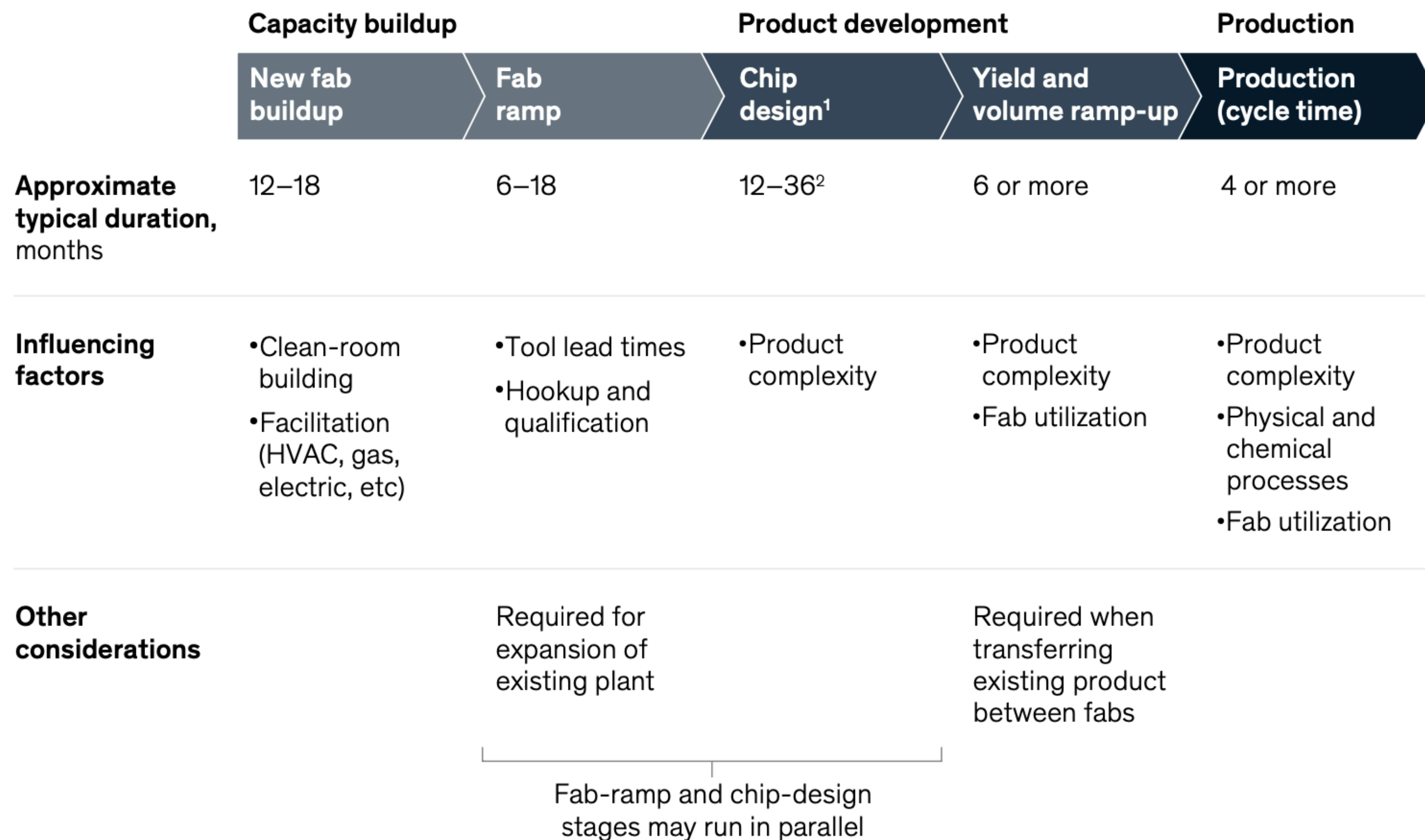
Lead times for semiconductor production can exceed four months, while switching to a new manufacturer takes a year or longer.

Semiconductor development and production timelines



[1]Chip design can be driven independent of fab manufacturing capacity.
[2]Eg, ~12-month product lifecycle for mobile phones; 24–36-month development time for automotive microcontroller units.
Source: McKinsey analysis

Over the past two decades, semiconductor capacity increased by an average of 4 percent a year, while utilization has remained high.

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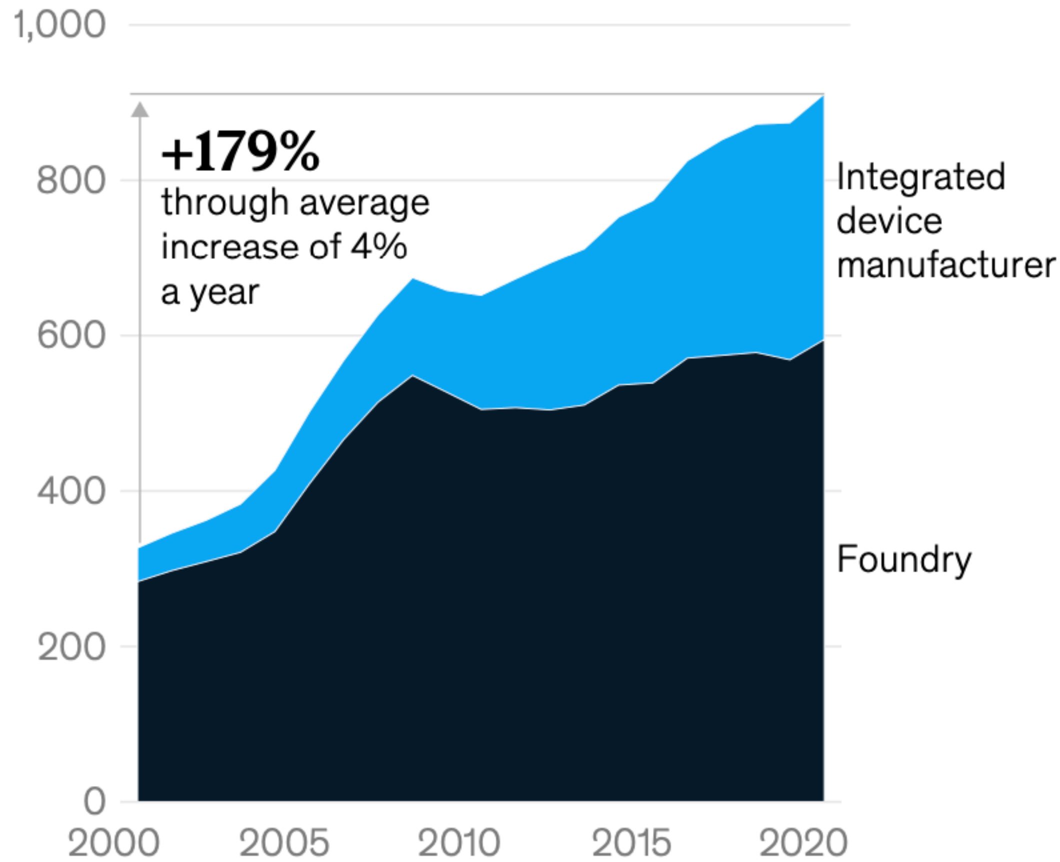
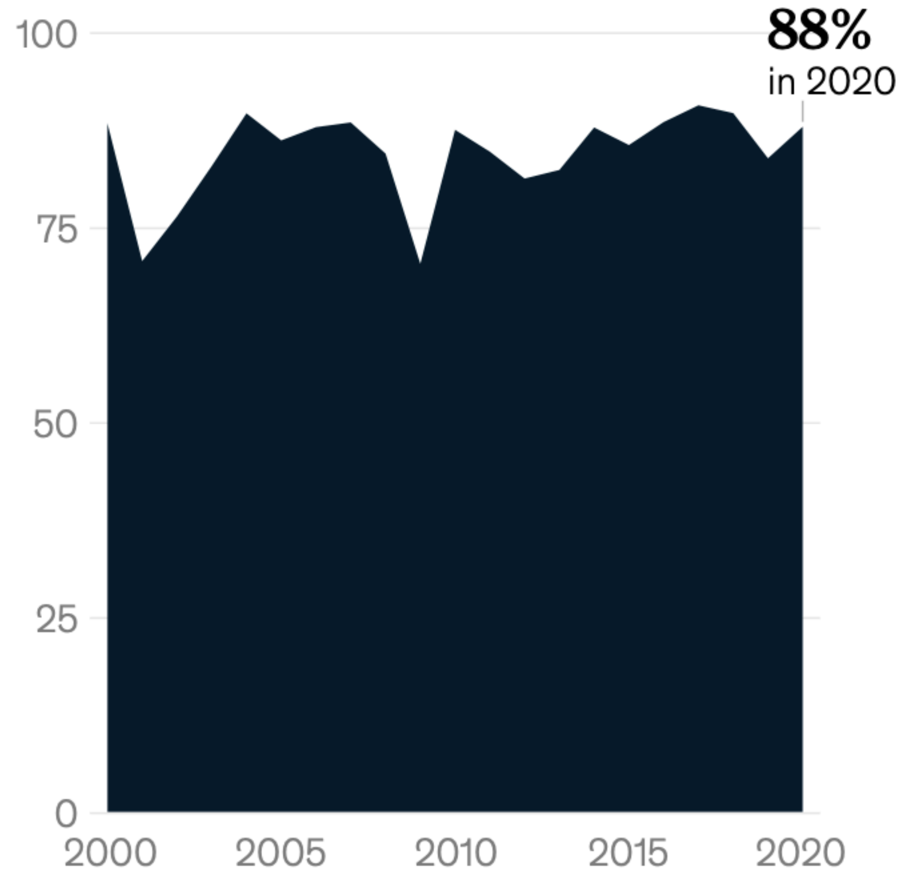
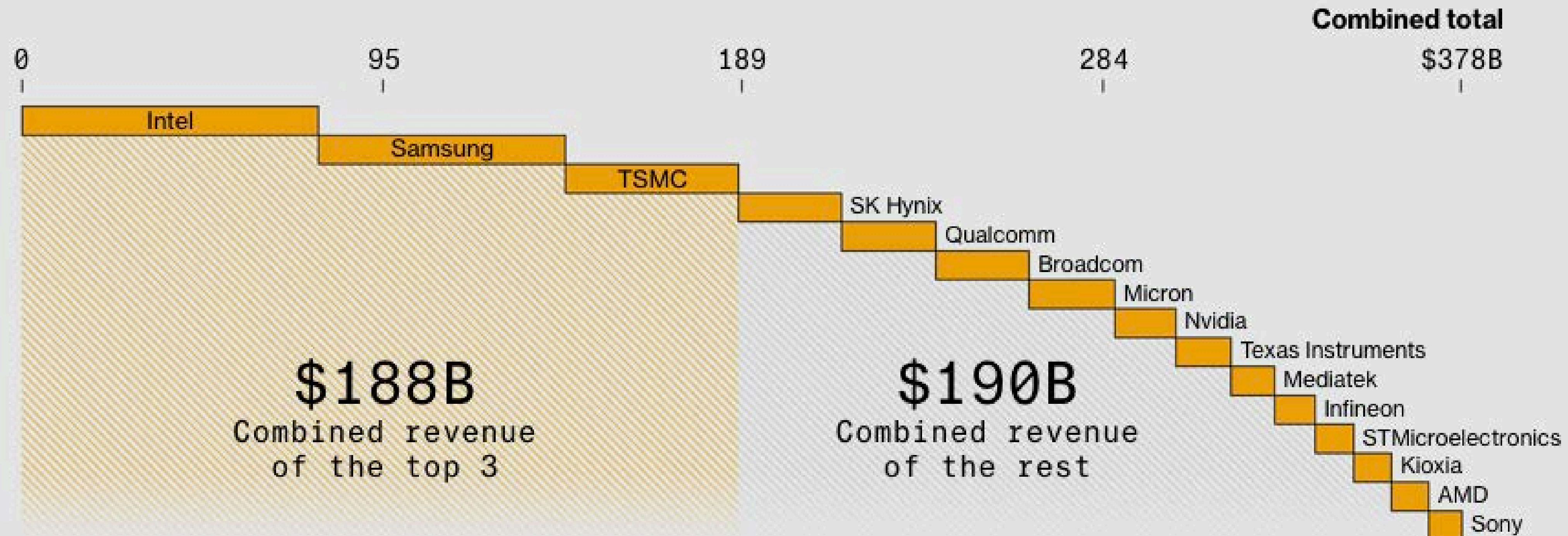
Semiconductor production capacity, million square inches per month



Semiconductor production capacity utilization, %



Source: IHS-Omdia; McKinsey analysis



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OEM - ODM - EMS

2020 Rank	2019 Rank	Company	2020 Revenue	2020 Market Share (%)	2019 Revenue	2019-2020 Growth (%)
1	1	Apple	53,616	11.9	43,239	24.0
2	2	Samsung Electronics	36,416	8.1	30,247	20.4
3	3	Huawei	19,086	4.2	24,933	-23.5
4	4	Lenovo	18,555	4.1	16,773	10.6
5	5	Dell Technologies	16,581	3.7	15,584	6.4
6	6	BBK Electronics	13,393	3.0	11,653	14.9
7	7	HP Inc.	10,992	2.4	10,729	2.4
8	8	Xiaomi	8,790	2.0	6,974	26.0
9	9	Hon Hai Precision Industry	5,730	1.3	5,816	-1.5
10	10	Hewlett Packard Enterprise	5,570	1.2	5,561	0.2
		Others	261,109	58.0	247,640	5.4
		Total	**449,838**	**100.0**	**419,148**	**7.3**

Vulnerabilità e recenti accadimenti

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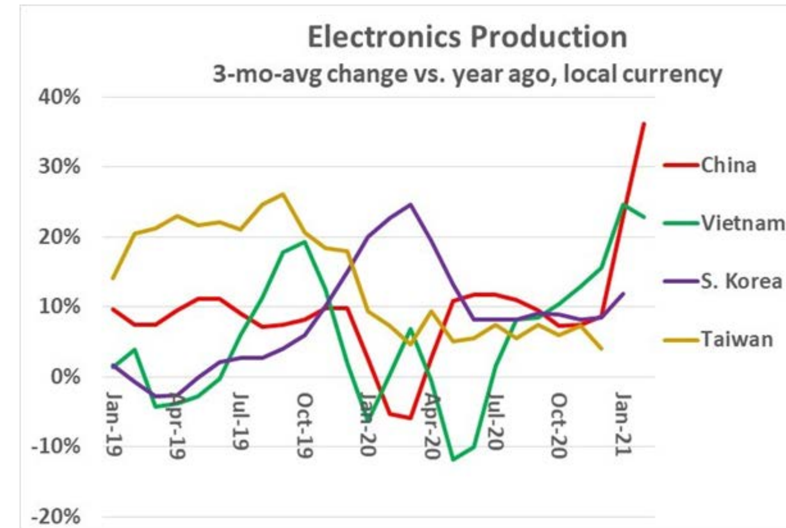
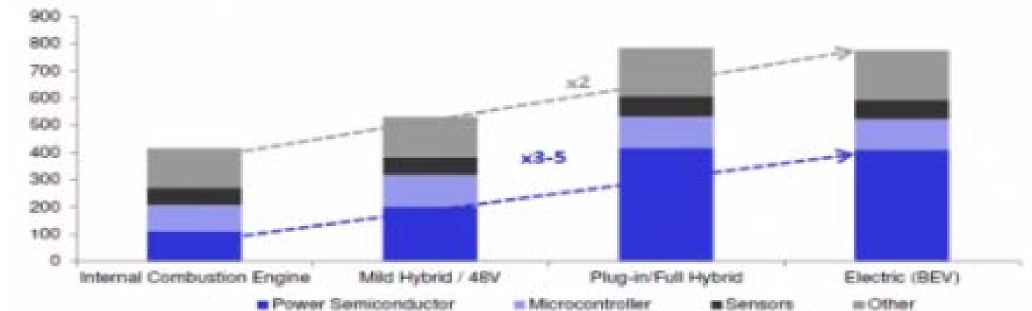
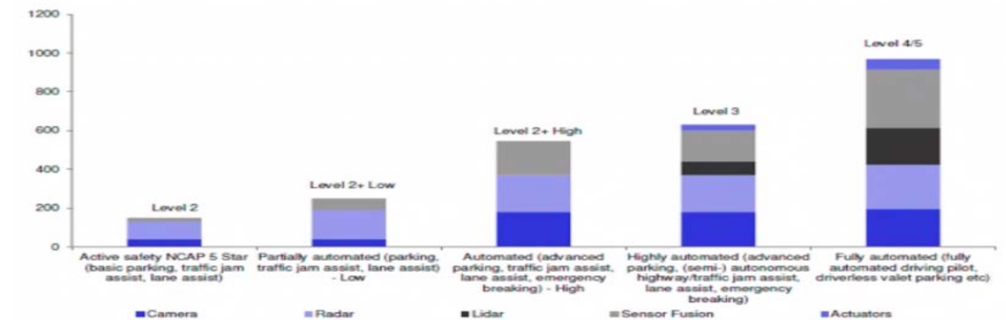
The Perfect Storm

- Demand Debounce after downturn
- Relentless Pervasivity
- Raw Material Price Increase
- Earthquakes, Tsunami, Fires
- Inclement Weather
- Transportation Disruption
- Trade Wars and Strategic Investments







L’innovazione e la progettazione:
il paradosso Lego sull’integrazione e specializzazione

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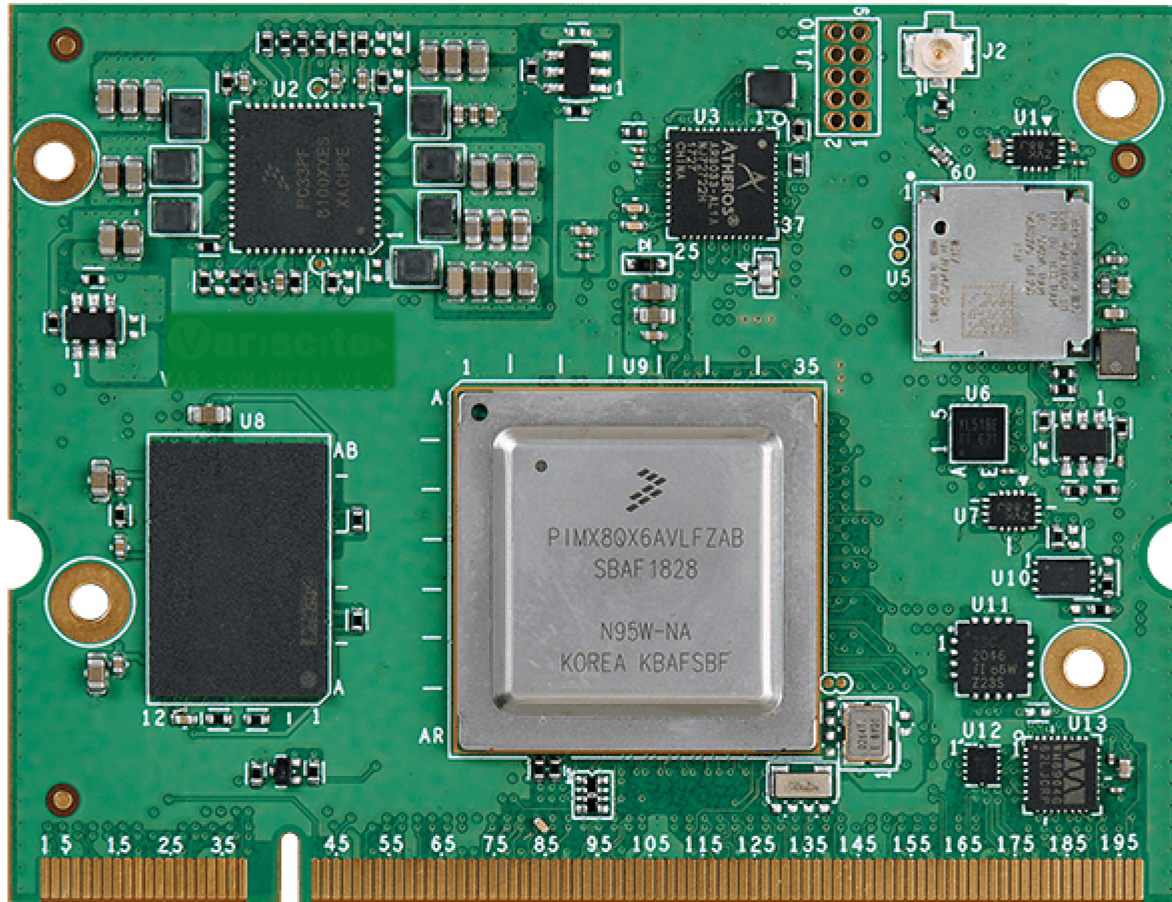
PIMX8QX6AVLFZAB
SBAF1828
N95W-NA
KOREA KBAFSBF

DIGITAL - PWM~
UNO
ARDUINO
POWER
ANALOG IN
A0 A1 A2 A3 A4 A5

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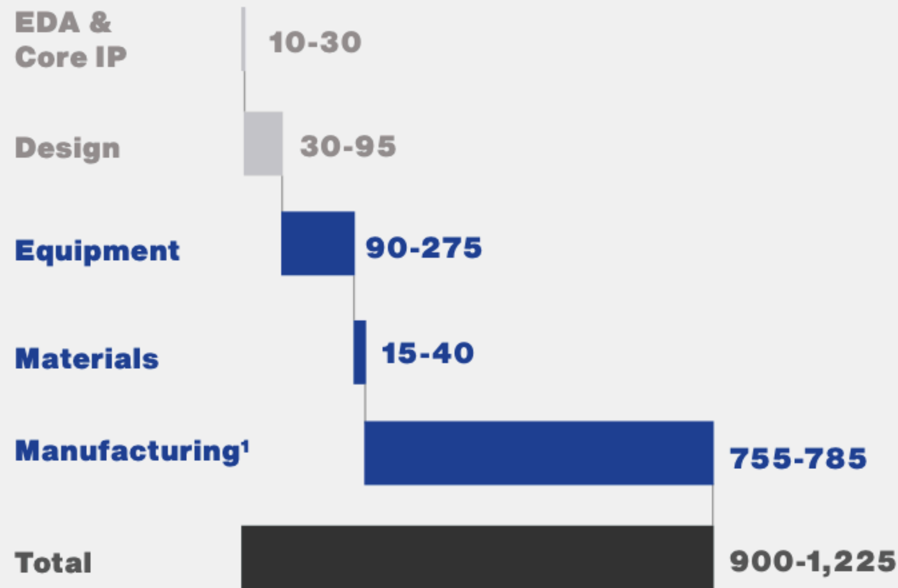
Autosufficienza: risorse economiche, temporali ed umane

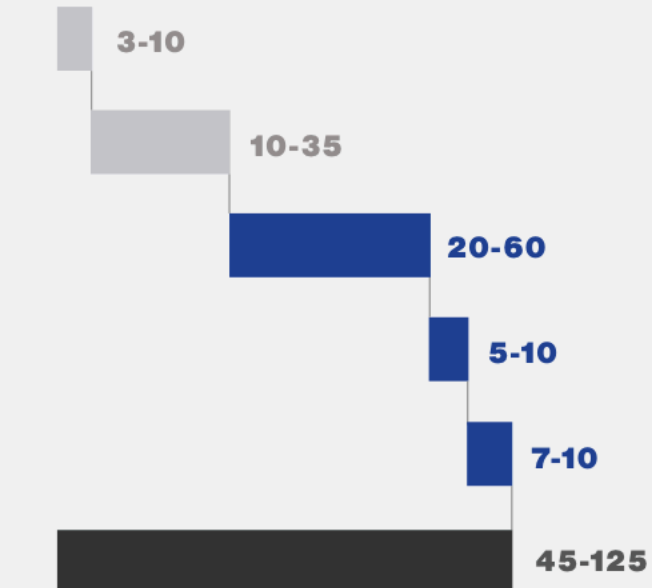
The staggering cost of hypothetical semiconductor self-sufficiency

Incremental cost to cover 2019 demand with fully "self-sufficient" localized semiconductor supply chains

Upfront investment ($ Billion)



Incremental annual cost ($ Billion)



Design   Manufacturing

1. Including both wafer fabrication and assembly, packaging and testing
Note: Range defined primarily by number of local companies assumed to be required to meet the local needs in each activity of the value chain: from just 1 player to supply the entire local market to 3 players typically found in the current global market structure
Sources: BCG analysis

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All regions benefit from the efficiencies of the global semiconductor supply chain

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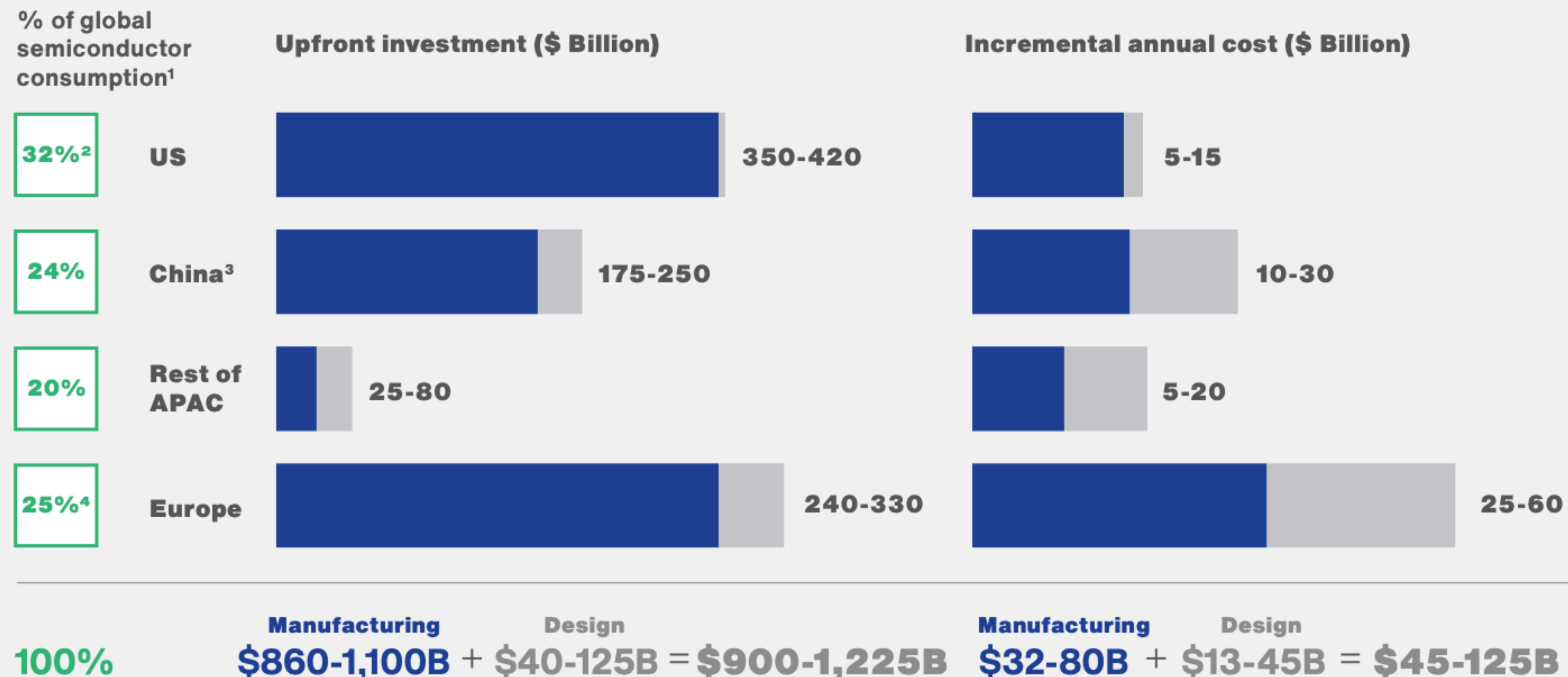

1. Calculated as the estimated semiconductor content in electronic devices sold to end users in each geography in 2019 2. Includes Canada, Latin America 3. Mainland China 4. Includes Middle East and Africa
Note: Range defined primarily by number of local companies assumed to be required to meet the local needs in each activity of the value chain: from just 1 player to supply the entire local market to 3 players typically found in the current global market structure
Sources: BCG analysis

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Proteggersi della situazione congiunturale

Ingegneria dei componenti

- Nel mercato industriale poche aziende hanno volumi rilevanti a livello del singolo part number
- La maggior parte delle produzioni sono «high mix, low volume»
- I criteri di selezione dei componenti hanno effetti sul TCO sul medio e lungo termine (obsolescenza e disponibilità)
- Rinnovare le tecnologie mature con quelle equivalenti più recenti
- Selezionare prodotti industriali a larga diffusione e multipurpose rispetto a prodotti consumer estremamente ottimizzati
- Priorità a package standard rispetto a quelli consumer
- Ottimizzare i volumi per contenere i costi

Ottimizzazione della Supply Chain

- La partership con il proprio fornitore è strategica
- Estendere il proprio portafoglio ordini per allocare capacità produttiva
- Condividere il rischio: strumenti di gestione del backlog
- Modularizzare il proprio prodotto per ridurre l'impatto della supply chain
- Ridondare i progetti per crearsi delle alternative anche su prodotti proprietari
  - Supersets, diebanks, packages

- La situazione potrebbe peggiorare prima di migliorare